

C2
cancel'd.

- (f) applying a treatment to the exposed portion of the SiC wafer surface, the treatment selected from a group consisting of chemical cleaning, surface etching and ion implantation; and
- (g) implanting an edge termination layer into the wafer beneath the surface of the insulating layer but not beneath the conductive material.

REMARKS

Claims 19 and 20 have been canceled. Claims 1 and 18 have been amended.

Claims 1, 3-8 and 18 are pending.

CLAIM REJECTION UNDER 35 USC § 103

The Examiner rejected claims 1-6, 8 and 18-20 under 35 USC § 103(a) as being unpatentable over Lillienfeld et al. in combination with Baliga et al., as previously applied in the Office Action dated October 2, 2002, and Cox et al. Claims 19 and 20 have been canceled. (The Applicant notes that Claim 2 was previously canceled.) As regards Lillienfeld et al. and Baliga et al., the Applicant respectfully submits that the two references do not combine to disclose the invention of independent claim 1 as contended in the October 2, 2002 Office Action.

The Examiner contends that Baliga et al. includes forming contact 14 on surface 22 of silicon wafer 12 (Col. 4, lines 10-12 and Fig. 1A), and then implanting inert ion such as argon ions (Col. 3, lines 26-27, Col 7, lines 41-42 and Fig. 1B), thereby forming termination region 16 (Col. 4, lines 30-33, Fig. 1C). (Office Action, 10/02/02, Page 4). The Examiner concedes that Lillienfeld et al. does not teach the step of implanting edge termination layer beneath the wafer surface. (Office Action, 10/02/02, Page 4).

Claim 1, as amended, clearly claims implanting an edge termination layer into the wafer beneath the surface of the insulating layer but not beneath the conductive material. Referring to the preferred embodiment of the present invention, edge termination layer 32 (32a, 32b, 32c) is formed on SiC wafer 20 but beneath first oxide layer 22 (22a, 22b, 22c), and optionally beneath second oxide layer 36 (36a, 36b, 36c). (Pages 6 and 7, Figs. 2F, 2G and 2H). This results in the advantages of reducing electric field crowding and improved protection against surface damage. Claim 18, as amended, also specifically claims implanting an edge termination layer into the wafer beneath the surface of the insulating layer but not beneath the conductive material.

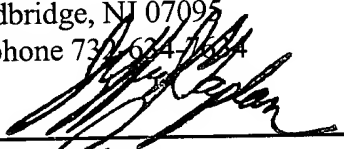
Lillienfeld et al. does not teach the step of implanting edge termination layer beneath the wafer surface. Baliga et al. discloses its termination region 16 forming on the surface 22 of silicon wafer 12, beneath nothing. Baliga et al. does not teach toward implanting an edge termination layer into the wafer beneath the surface of an insulting layer but not beneath conductive material. As neither Baliga et al. nor Lillienfeld et al. teach an element of the present invention, claim 1 and claim 18 cannot be obvious in light of Lillienfeld et al. in combination with Baliga et al. Claims 3-6 and 8 are dependent upon claim 1, which for the above-stated reasons the Applicant submits is allowable. Therefore, the Applicant respectfully submits that claims 1, 3-6, 8 and 18 should be allowed.

The Examiner rejected claim 7 under 35 USC § 103(a) as being unpatentable over Lillienfeld et al. in combination with Baliga et al. and Cox et al., and in further view of Thero et al. Claim 7 is dependent upon claim 1, which for the reasons stated above regarding Lillienfeld et al. and Baliga et al., the Applicant submits is allowable. Therefore, the Applicant respectfully submits that claim 7 should be allowed.

In view of the foregoing amendment and remarks, it is respectfully submitted that all claims pending are allowable. Therefore, reconsideration and allowance are respectfully requested.

Respectfully submitted,

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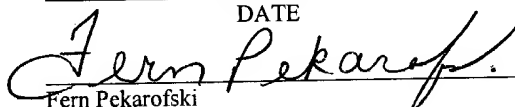


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